

MPC102

Wide-Bandwidth DIFFERENTIAL 2 x 1 MULTIPLEXER

FEATURES

- **BANDWIDTH:** 210MHz (1.4Vp-p)
- **LOW INTERCHANNEL CROSSTALK:**
-68dB (30MHz, SO); -58dB (30MHz, DIP)
- **LOW SWITCHING TRANSIENTS:**
+6mV/-8mV
- **LOW DIFFERENTIAL GAIN/PHASE ERRORS:** 0.02%, 0.02°
- **LOW QUIESCENT CURRENT:**
One Channel Selected: $\pm 4.6\text{mA}$
No Channel Selected: $\pm 250\mu\text{A}$

APPLICATIONS

- **VIDEO ROUTING AND MULTIPLEXING (CROSSPOINTS)**
- **RADAR SYSTEMS**
- **DATA ACQUISITION**
- **DISC R/W TEST SYSTEMS**
- **xDSL TEST SYSTEMS**

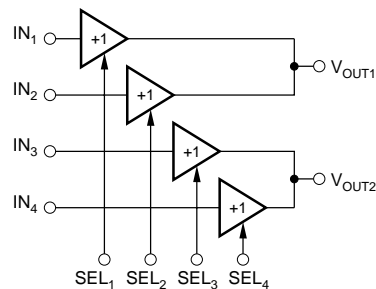
DESCRIPTION

The MPC102 is dual, wide-bandwidth, differential 2-to-1 multiplexer, which can be used in a wide variety of applications.

It was designed for wide-bandwidth systems, including high-definition television and broadcast equipment. Although it is primarily used to route video signals, the harmonic and dynamic attributes of the MPC102 also make it appropriate for other analog signal routing applications such as radar, communications, computer graphics, and data acquisition systems.

The MPC102 consists of four identical monolithic, integrated, open-loop buffer amplifiers. Two buffer outputs are each connected internally at the output. The bipolar complementary buffers form a unidirectional transmission path and offer extremely high output-to-input isolation. The MPC102 multiplexer enables the user to connect one of two input signals to the corresponding output. The output of the multiplexer is in a high-impedance state when no channel is selected. When one channel is selected with a digital "1" at the corresponding SEL input, the component acts as a buffer with high input impedance and low output impedance.

The wide bandwidth of over 210MHz at 1.4Vp-p signal level, high linearity and low distortion, and low input voltage noise of $4\text{nV}/\sqrt{\text{Hz}}$ make this crosspoint switch suitable for RF and video applications. All performance is specified with $\pm 5\text{V}$ supply voltage, which reduces power consumption in comparison with $\pm 15\text{V}$ designs. The multiplexer is available in a space-saving SO-14 and DIP packages. Both are designed and specified for operation over the industrial temperature range (-40°C to $+85^\circ\text{C}$.)



TRUTH TABLE

SEL ₁	SEL ₂	SEL ₃	SEL ₄	V _{OUT1}	V _{OUT2}
0	0	0	0	HI-Z	HI-Z
1	0	0	0	IN ₁	HI-Z
0	1	0	0	IN ₂	HI-Z
0	0	1	0	HI-Z	IN ₃
0	0	0	1	HI-Z	IN ₄

SPECIFICATIONS

ELECTRICAL

At $V_{CC} = \pm 5V$, $R_L = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU			UNITS
		MIN	TYP	MAX	
DC CHARACTERISTICS					
INPUT OFFSET VOLTAGE	$R_{IN} = 0$, $R_{SOURCE} = 0$				
Initial			14	± 30	mV
vs Temperature			60		$\mu V/^\circ C$
vs Supply (Tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$	-40	-74		dB
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		-50		dB
vs Supply (Non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		-50		dB
Initial Matching	All Four Buffers		± 3		mV
INPUT BIAS CURRENT					
Initial			4	± 10	μA
vs Temperature			20		$nA/^\circ C$
vs Supply (Tracking)	$V_{CC} = \pm 4.5V$ to $\pm 5.5V$		± 710		nA/V
vs Supply (Non-tracking)	$V_{CC} = +4.5V$ to $+5.5V$		0.26		$\mu A/V$
vs Supply (Non-tracking)	$V_{CC} = -4.5V$ to $-5.5V$		1.7		$\mu A/V$
INPUT IMPEDANCE					
Resistance	Channel On		0.88		M Ω
Capacitance	Channel On		1.0		pF
Capacitance	Channel Off		1.0		pF
INPUT NOISE					
Voltage Noise Density	$f_{OUT} = 20kHz$ to $10MHz$		4.0		nV/\sqrt{Hz}
Signal-to-Noise Ratio	$S/N = 0.7/(V_{IN} \cdot \sqrt{5MHz})$		98		dB
INPUT VOLTAGE RANGE	Gain Error $\leq 10\%$		± 3.6		V
TRANSFER CHARACTERISTICS					
Voltage Gain	$R_L = 1k\Omega$, $V_{IN} = \pm 2V$		0.982		V/V
Voltage Gain	$R_L = 10k\Omega$, $V_{IN} = \pm 2.8V$	0.98	0.992		V/V
RATED OUTPUT					
Voltage	$V_{IN} = \pm 3V$, $R_L = 10k\Omega$	± 2.8	± 2.98		V
Resistance	One Channel Selected		11		Ω
Resistance	No Channel Selected		900		M Ω
Capacitance	No Channel Selected		1.5		pF
CHANNEL SELECTION INPUTS					
Logic 1 Voltage		+2		V_{CC}	V
Logic 0 Voltage				+0.8	V
Logic 1 Current	$V_{SEL} = 5.0V$		100	150	μA
Logic 0 Current	$V_{SEL} = 0.8V$			5	μA
SWITCHING CHARACTERISTICS					
SEL to Channel ON Time	$V_{IN} = -0.3V$ to $+0.7V$, $f = 5MHz$		0.25		μs
SEL to Channel OFF Time	90% Point of $V_{OUT} = 1Vp-p$		0.25		μs
Switching Transient, Positive	10% Point of $V_{OUT} = 1Vp-p$		6		mV
Switching Transient, Negative	Measured While Switching Between Two Grounded Channels		-8		mV
POWER SUPPLY					
Rated Voltage			± 5		V
Derated Performance		± 4.5		± 5.5	V
Quiescent Current	One Channel Selected		± 4.6	± 5	mA
	No Channel Selected		± 250	± 350	μA
Rejection Ratio			-80		dB
TEMPERATURE RANGE					
Operating		-40		+85	$^\circ C$
Storage		-40		+125	$^\circ C$
Thermal Resistance, θ_{JA}			90		$^\circ C/W$

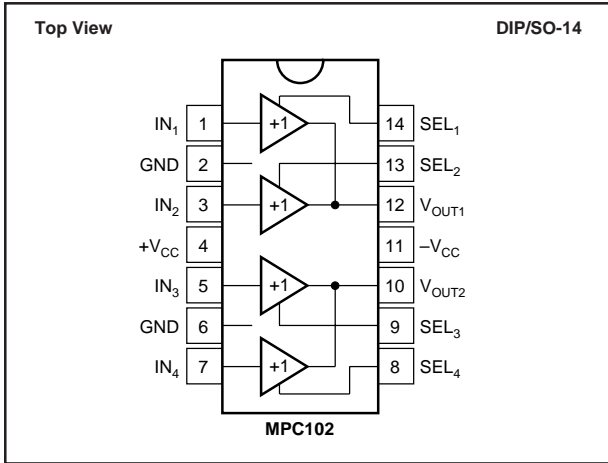
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SPECIFICATIONS—AC CHARACTERISTICS (CONT)

At $V_{CC} = \pm 5V$, $R_L = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25^\circ C$, unless otherwise noted.

PARAMETER	CONDITIONS	MPC102AP, AU			UNITS
		MIN	TYP	MAX	
LARGE SIGNAL BANDWIDTH (-3dB)	$V_{OUT} = 5.0V_{p-p}$, $C_{OUT} = 1pF$		55		MHz
	$V_{OUT} = 2.8V_{p-p}$, $C_{OUT} = 1pF$		100		MHz
	$V_{OUT} = 1.4V_{p-p}$, $C_{OUT} = 1pF$		210		MHz
SMALL SIGNAL BANDWIDTH	$V_{OUT} = 0.2V_{p-p}$, $C_{OUT} = 1pF$		370		MHz
GROUP DELAY TIME			450		ps
DIFFERENTIAL GAIN	$f = 4.43MHz$, $V_{IN} = 0.3V_{p-p}$ $VDC = 0$ to $0.7V$		0.02		%
DIFFERENTIAL PHASE	$f = 4.43MHz$, $V_{IN} = 0.3V_{p-p}$ $VDC = 0$ to $0.7V$		0.02		Degrees
GAIN FLATNESS PEAKING	$V_{OUT} = 0.2V_{p-p}$, DC to 30MHz		0.04		dB
	$V_{OUT} = 0.2V_{p-p}$, DC to 100MHz		0.05		dB
HARMONIC DISTORTION	$f = 30MHz$, $V_{OUT} = 1.4V_{p-p}$, $R_L = 350\Omega$		-64		dBc
			-66		dBc
CROSSTALK	MPC102AP Channel-to-Channel	$V_{IN} = 1.4V_{p-p}$ $f = 5MHz$,		-75	dB
		$f = 30MHz$,		-58	dB
	Off Isolation	$f = 5MHz$,		-70	dB
		$f = 30MHz$,		-71	dB
	MPC102AU Channel-to-Channel	$f = 5MHz$,		-78	dB
		$f = 30MHz$,		-68	dB
Off Isolation	$f = 5MHz$,		-75	dB	
	$f = 30MHz$		-76	dB	
TIME DOMAIN					
RISE/FALL TIME	$V_{OUT} = 1.4V_{p-p}$, Step 10% to 90% $C_{OUT} = 1pF$, $R_{OUT} = 22\Omega$		2.5		ns
SLEW RATE	$V_{OUT} = 1.4V_{p-p}$ $C_{OUT} = 1pF$ $C_{OUT} = 22pF$ $C_{OUT} = 47pF$		500		$V/\mu s$
			360		$V/\mu s$
			260		$V/\mu s$
					$V/\mu s$

CONNECTION DIAGRAM



PIN DESCRIPTION

PIN	DESCRIPTION
IN ₁ , IN ₂	Analog Inputs Channel 1 and 2
IN ₃ , IN ₄	Analog Inputs Channel 3 and 4
GND	Analog Shielding Grounds, Connect to System Ground
SEL ₁ , SEL ₂	Channel Selection Inputs
V _{OUT1}	Analog Output 1
V _{OUT2}	Analog Output 2
-V _{CC}	Negative Supply Voltage; typical -5VDC
+V _{CC}	Positive Supply Voltage; typical +5VDC



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage ($\pm V_{CC}$)	$\pm 6V$
Analog Input Voltage (IN ₁ through IN ₄)	$\pm V_{CC}$, $\pm 0.7V$
Operating Temperature	-40°C to +85°C
Storage Temperature	-40°C to +125°C
Output Current	$\pm 6mA$
Junction Temperature	+175°C
Lead Temperature (soldering, 10s)	+300°C
Digital Input Voltages (SEL ₁ through SEL ₄)	-0.5V to +V _{CC} +0.7V
Logic Voltage Input	-0.6V to +V _{CC} +0.6V

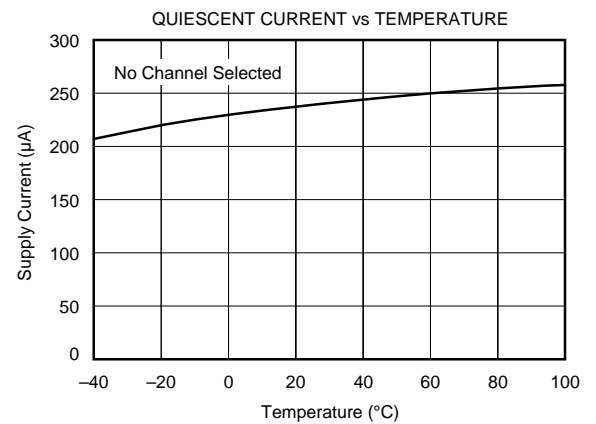
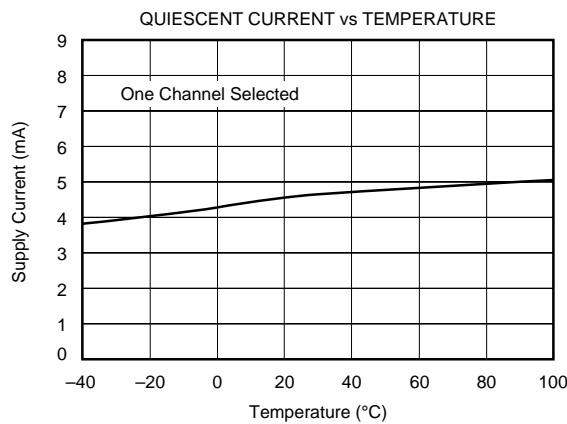
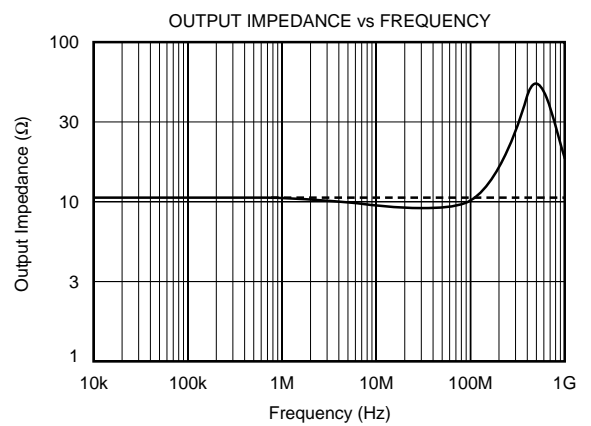
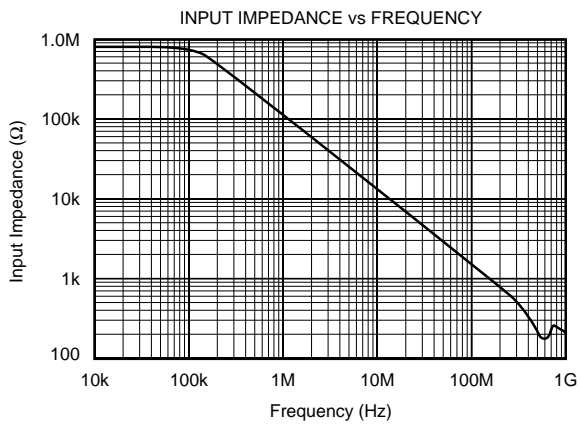
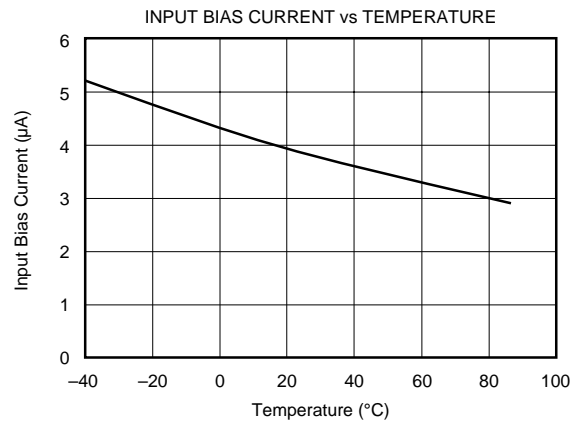
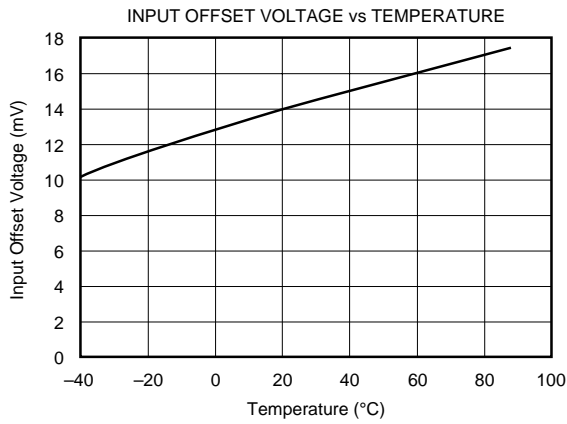
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER ⁽¹⁾	TEMPERATURE RANGE
MPC102AP	14-Pin DIP	010	-40°C to +85°C
MPC102AU	SO-14 Surface Mount	235	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

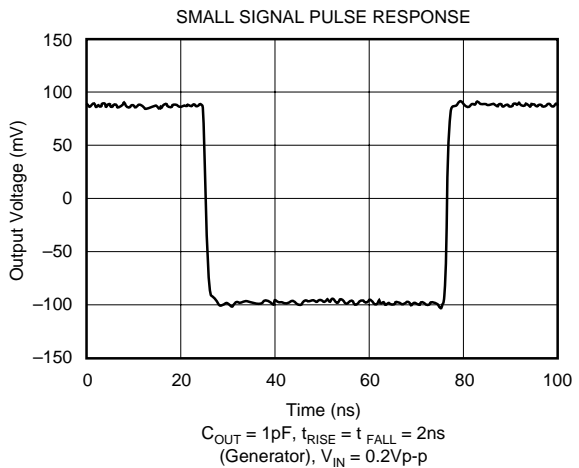
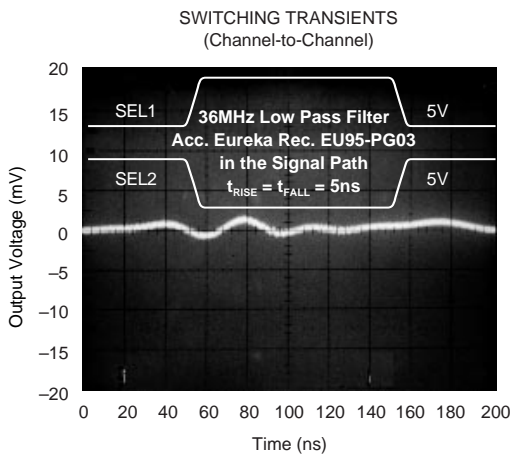
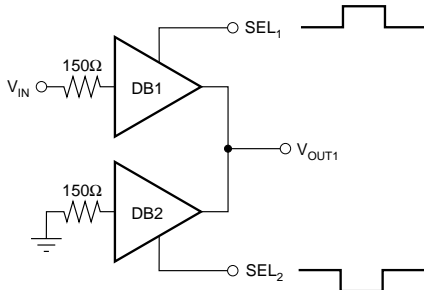
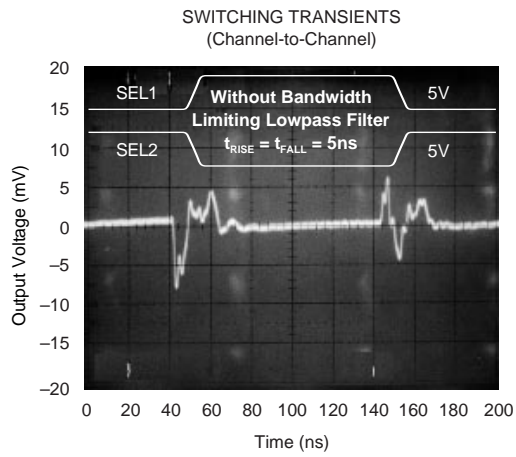
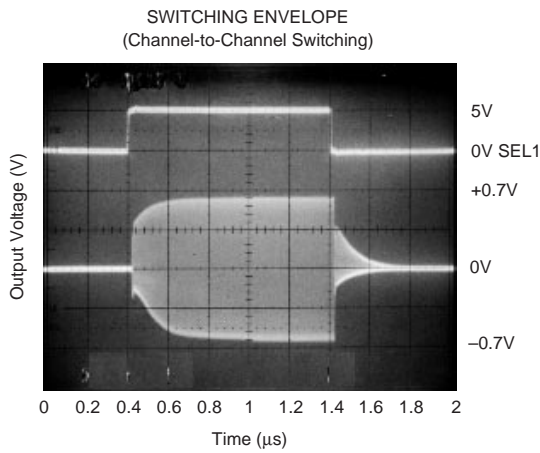
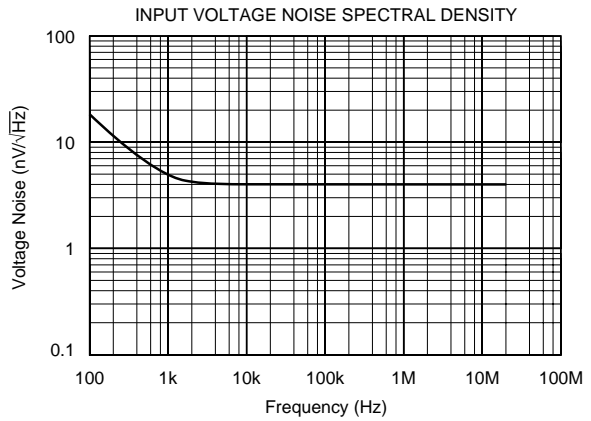
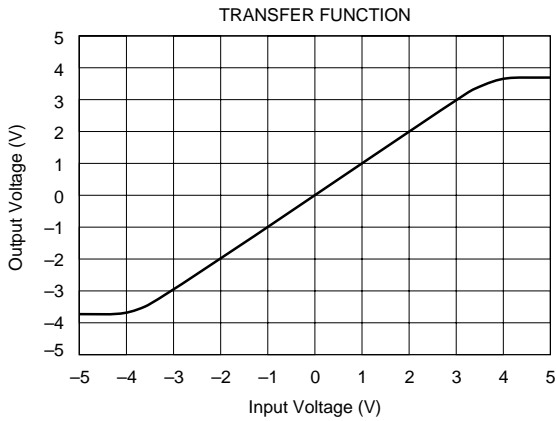
TYPICAL PERFORMANCE CURVES

At $V_{CC} = \pm 5V$, $R_{LOAD} = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25^\circ C$, unless otherwise noted.



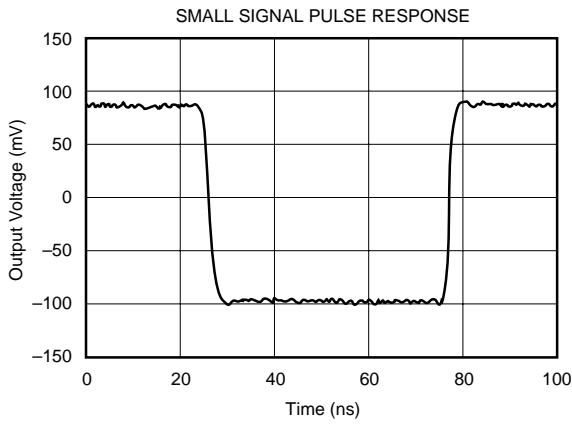
TYPICAL PERFORMANCE CURVES (CONT)

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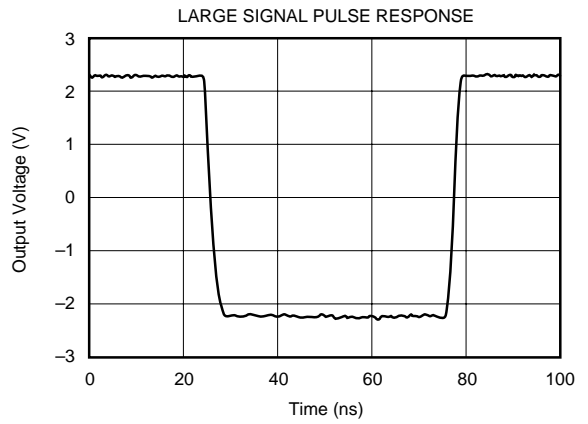


TYPICAL PERFORMANCE CURVES (CONT)

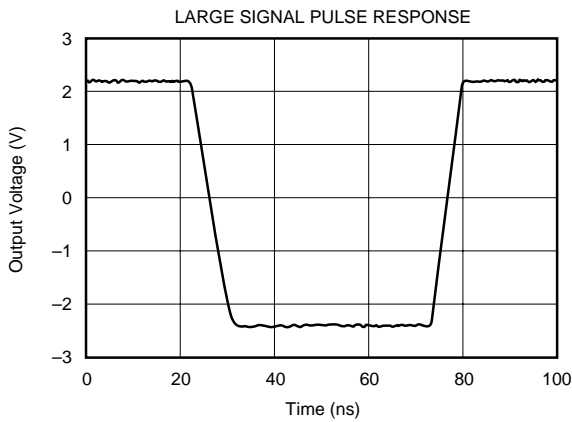
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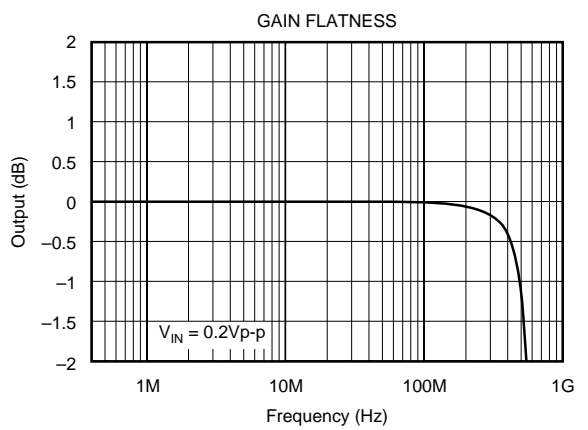
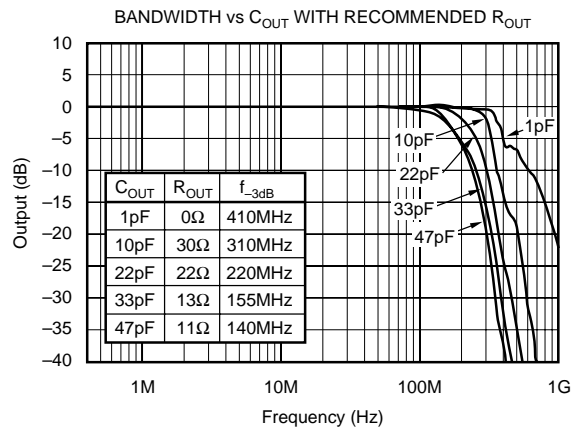
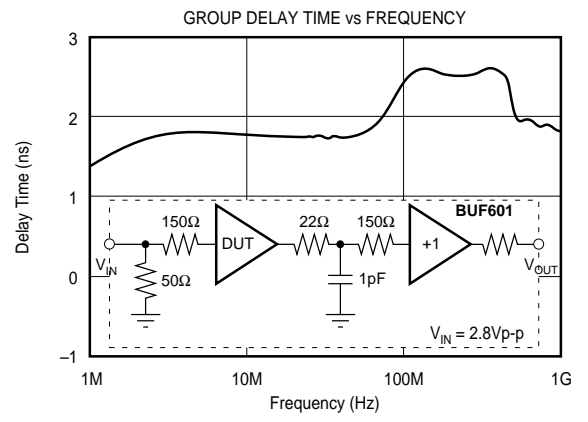
$C_{OUT} = 47pF$, $t_{RISE} = t_{FALL} = 2ns$
(Generator), $V_{IN} = 0.2Vp-p$



$C_{OUT} = 1pF$, $t_{RISE} = t_{FALL} = 5ns$
(Generator), $V_{IN} = 5Vp-p$

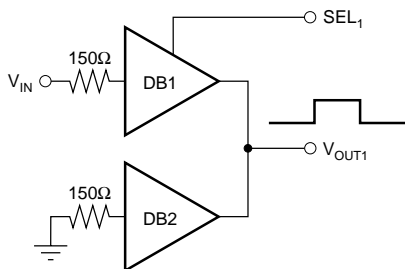
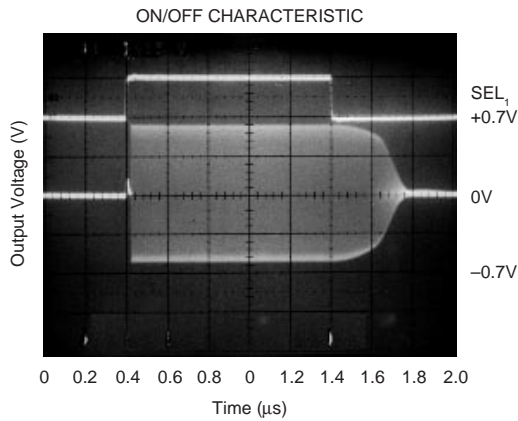
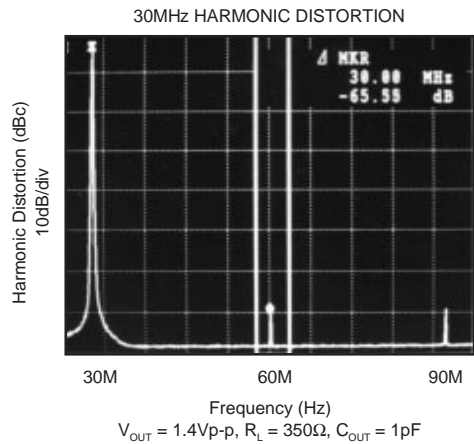
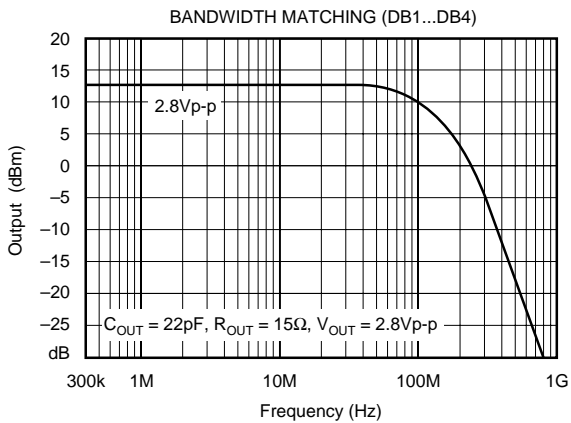
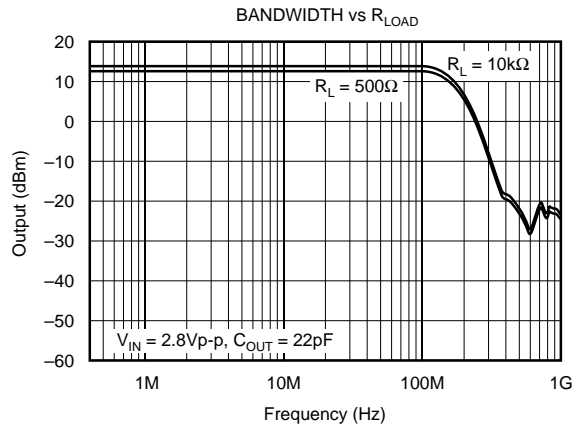
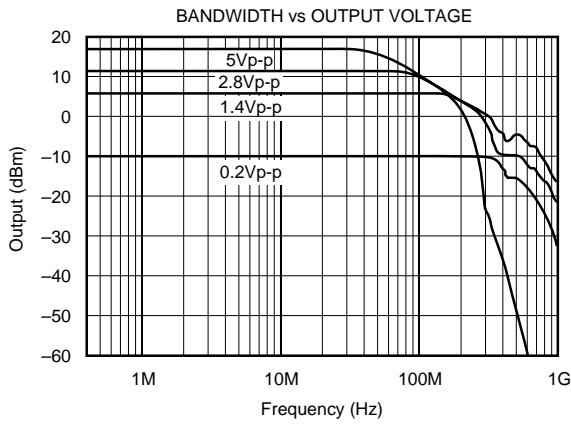


$C_{OUT} = 47pF$, $t_{RISE} = t_{FALL} = 5ns$
(Generator), $V_{IN} = 5Vp-p$



TYPICAL PERFORMANCE CURVES (CONT)

At $V_{CC} = \pm 5V$, $R_{LOAD} = 10k\Omega$, $R_{IN} = 150\Omega$, $R_{SOURCE} = 50\Omega$, and $T_A = +25^\circ C$, unless otherwise noted.



APPLICATIONS INFORMATION

The MPC102 operates from $\pm 5V$ power supplies ($\pm 6V$ maximum). Do not attempt to operate with larger power supply voltages or permanent damage may occur. The buffer outputs are not current-limited or protected. If the output is shorted to ground, currents up to 18mA could flow. Momentary shorts to ground (a few seconds) should be avoided, but are unlikely to cause permanent damage.

INPUT PROTECTION

As shown below, all pins on the MPC102 are internally protected from ESD by a pair of back-to-back reverse-biased diodes to either power supply. These diodes will begin to conduct when the input voltage exceeds either power supply by about 0.7V. This situation can occur with loss of the amplifier's power supplies while a signal source is still present. The diodes can typically withstand a continuous current of 30mA without destruction. To insure long term reliability, however, diode current should be externally limited to 10mA whenever possible.

The internal protection diodes are designed to withstand 2.5kV (using Human Body Model) and will provide adequate ESD protection for most normal handling procedures. However, static damage can cause subtle changes in the characteristics of the buffer amplifier input without necessarily destroying the device. In precision buffer amplifiers, such damage may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the MPC102.

Static damage has been well-recognized as a problem for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. The MPC102 incorporates on-chip ESD protection diodes as shown in Figure 1. Thus the user does not need to add external protection diodes, which can add capacitance and degrade AC performance.

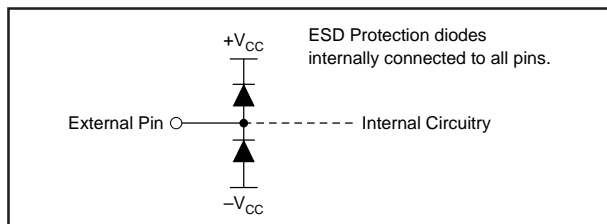


FIGURE 1. Internal ESD Protection.

DISCUSSION OF PERFORMANCE

The MPC102 is a dual, 2-to-1, wide-band analog signal multiplexer. It allows the user to connect one of the two inputs (IN_1/IN_2 or IN_3/IN_4) to the corresponding output. The switching speed between two input channels is typically less than 300ns.

However, in contrast to signal switches using CMOS or DMOS transistors, the switching transients are very low at

$+6mV$ and $-8mV$. The MPC102 consists of four identical unity-gain buffer amplifiers. Two of the four amplifiers are connected together internally at the output. The open-loop buffer amps, which consist of complementary emitter followers, apply no feedback so their low-frequency gain is slightly less than unity and somewhat dependent on loading. Unlike devices using MOS bilateral switching elements, the bipolar complementary buffers form a unidirectional transmission path, thus providing high output-to-input isolation. Switching stages compatible to TTL-level digital signals are provided for each buffer to select the input channel. When no channel is selected, the outputs of the device are high-impedance. This allows the user to wire several MPC102s together to create multichannel switch matrices.

Chip select logic is not integrated. The selected design increases the flexibility of address decoding in complex distribution fields, eases bus-controlled channel selection, simplifies channel selection monitoring for the user, and lowers transient peaks. All of these characteristics make the multiplexer, in effect, a quad switchable high-speed buffer. The buffers require DC coupling and termination resistors when driven directly from a low-impedance cable. High-current output amplifiers are recommended when driving low-impedance transmission lines or inputs.

An advanced complementary bipolar process, consisting of pn-junction isolated, high-frequency NPN and PNP transistors, provides wide bandwidth while maintaining low crosstalk and harmonic distortion. Bandwidth of over 210MHz at an output voltage of 1.4Vp-p allows the design of multi-channel crosspoint or distribution fields in HDTV-quality with an overall system bandwidth of 36MHz. The buffer amplifiers also offer low differential gain (0.02%) and phase (0.02°) errors. These parameters are essential for video applications and demonstrate how well the signal path maintains a constant small-signal gain and phase for the low-level color subcarrier at 4.43MHz (PAL) or 3.58MHz (NSTC) as the luminance signal is ramped through its specified range. The bipolar construction also ensures that the input impedance remains high and constant between ON and OFF states. The ON/OFF input capacitance ratio is near unity and does not vary with power supply voltage variations. The low output capacitance of 1.5pF when no channel is selected is a very important parameter for large distribution fields. Each parallel output capacitance is an additional load and reduces the overall system bandwidth.

Bipolar video crosspoint switches are virtually glitch-free when compared to signal switches using CMOS or DMOS devices. The MPC102 operates with a fast make-before-break switching action to keep the output switching transients small and short. Switching from one channel to another causes the signal to mix at the output for a short time, but it interferes minimally with the input signals. The transient peaks remain less than $+6mV$ and $-8mV$. The generated output transients are extremely small, so DC clamping during switching between channels is unnecessary. DC clamping during the switching dead time is required to avoid synchronization by large negative output glitches in subsequent equipment.

The SEL-to-channel-ON time is typically 25ns and is always shorter than the typical SEL-to-channel-OFF time of 250ns. In the worst case, an ON/OFF margin of 150ns ensures safe switching even for timing spreads in the digital control latches. The short interchannel switching time of 300ns allows channel change during the vertical blanking time, even in high-resolution graphic or broadcast systems. As shown in the typical performance curves, the signal envelope during transition from one channel to another rises and falls symmetrically and shows less overshooting and DC settling effects.

Power consumption is a serious problem when designing large crosspoint fields with high component density. Since most of the buffer amplifiers are in the off-state, one important design goal was to attain low off-state quiescent current when no channel is selected. The low supply current of $\pm 250\mu\text{A}$ when no channel is selected and $\pm 4.6\text{mA}$ when one channel is selected, as well as the reduced $\pm 5\text{V}$ supply voltage, conserves power, simplifies the power supply design, and results in cooler, more reliable operation.

CIRCUIT LAYOUT

The high-frequency performance of the MPC102 can be greatly affected by the physical layout of the circuit. The following tips are offered as suggestions, not as absolutes. Oscillations, ringing, poor bandwidth and settling, higher crosstalk, and peaking are all typical problems which plague high-speed components when they are used incorrectly.

- Bypass power supplies very close to the device pins. Use tantalum chip capacitors (approximately $2.2\mu\text{F}$), a parallel 470pF ceramic chip capacitor may be added if desired. Surface-mount types are recommended due to their low lead inductance.
- PC board traces for signal and power lines should be wide to reduce impedance.
- Make short and low inductance traces. The entire circuit layout should be as small as possible.
- Use a low-impedance ground plane on the component side to ensure that low-impedance ground is available throughout the layout. Grounded traces between the input traces are essential to achieve high interchannel crosstalk rejection.
- Do not extend the ground plane under high-impedance nodes sensitive to stray capacitances, such as the buffer's input terminals.
- Sockets are not recommended, because they add significant inductance and parasitic capacitance. If sockets are required, use zero-profile solderless sockets.
- Use low-inductance and surface-mounted components for best ac-performance.
- A resistor (100Ω to 200Ω) in series with the input of the buffers may help to reduce peaking. Place the resistor as close as possible to the pin.
- Plug-in prototype boards and wire-wrap boards will not function well. A clean layout using RF techniques is essential.

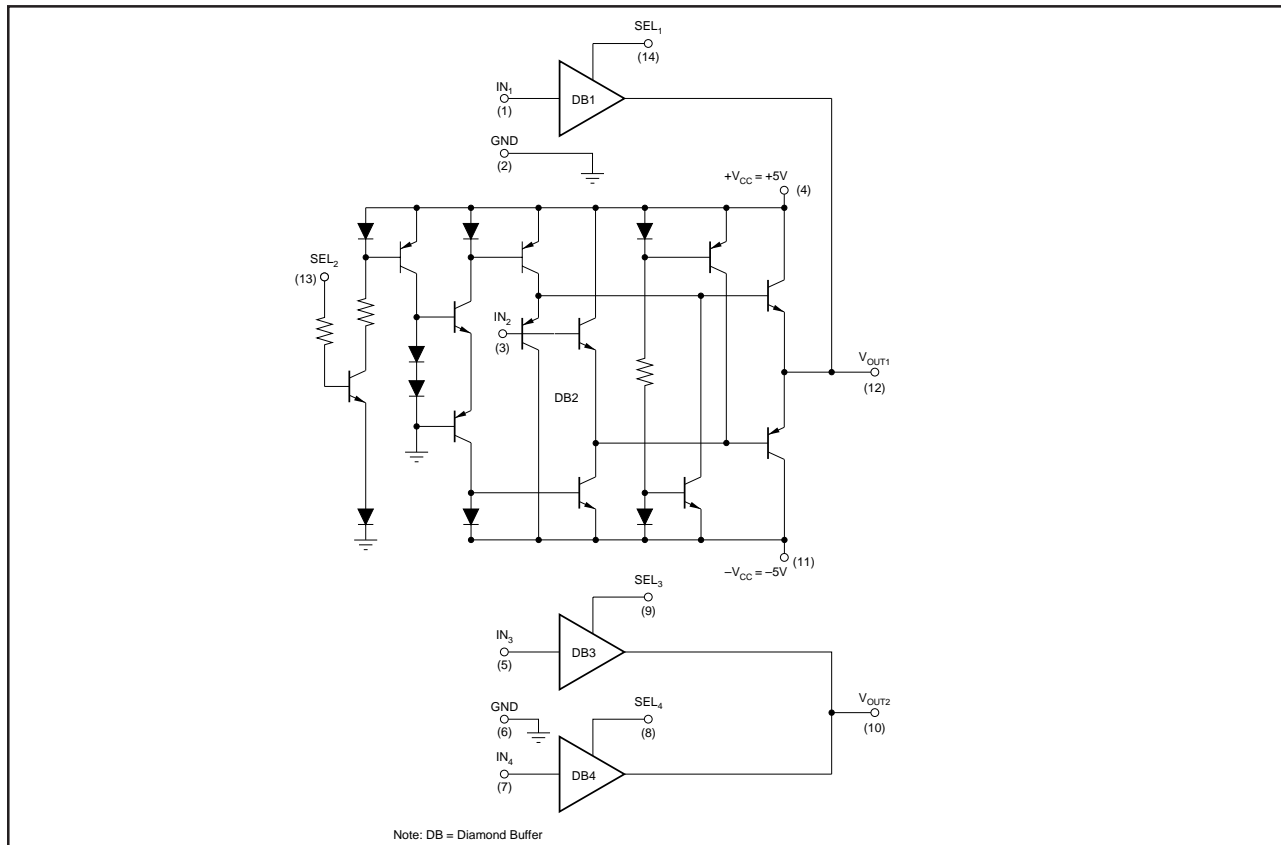


FIGURE 2. Simplified Circuit Diagram.

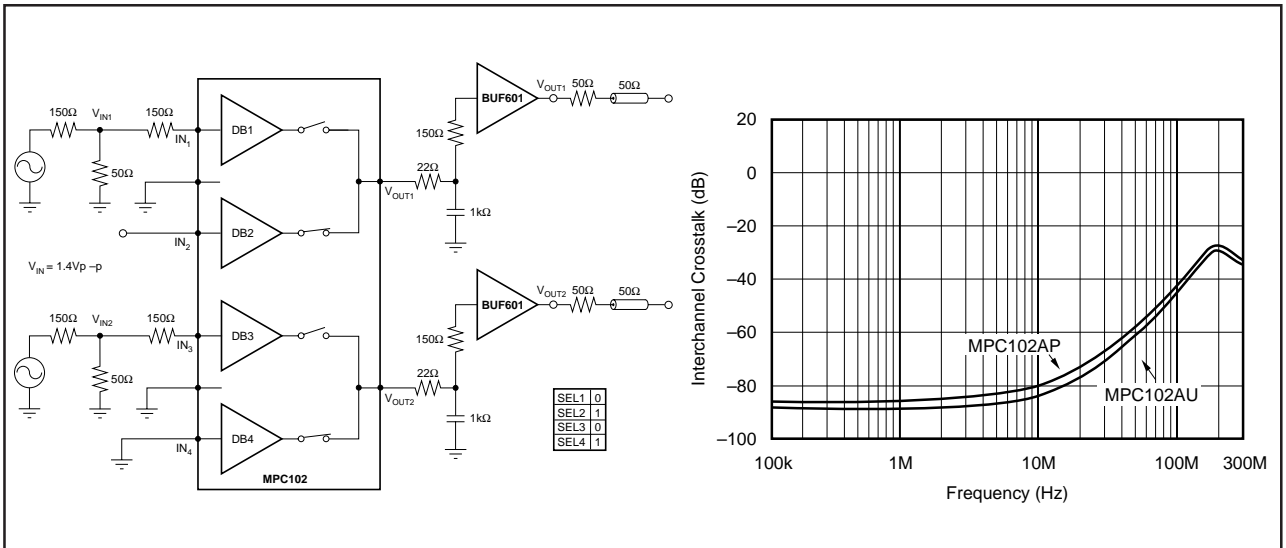


FIGURE 3. Channel Crosstalk – Grounded Input.

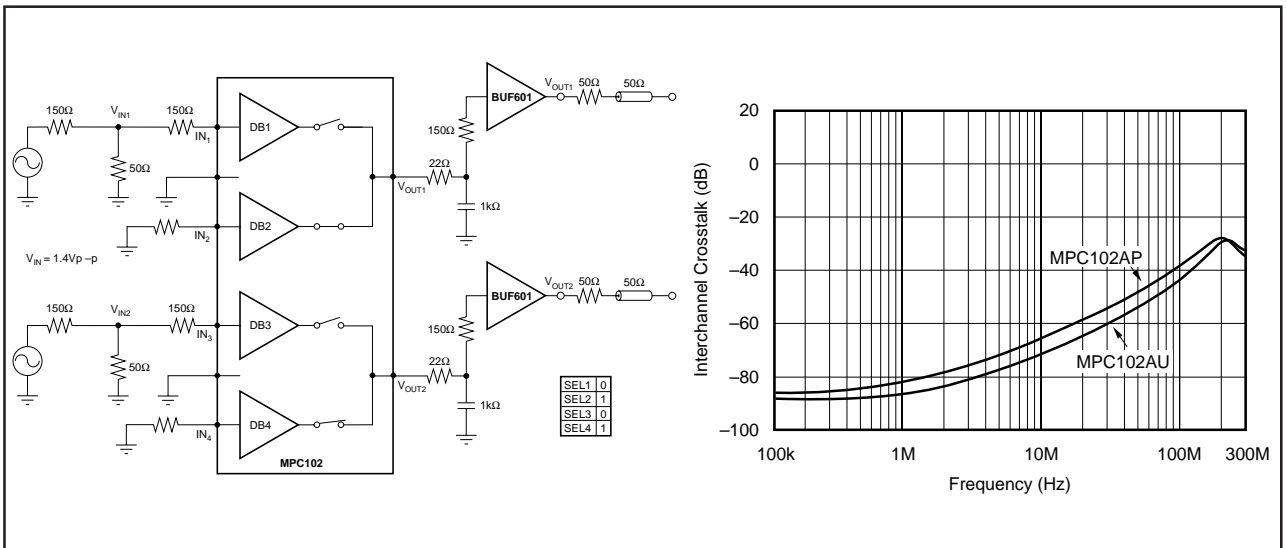


FIGURE 4. Off Isolation 150Ω Input.

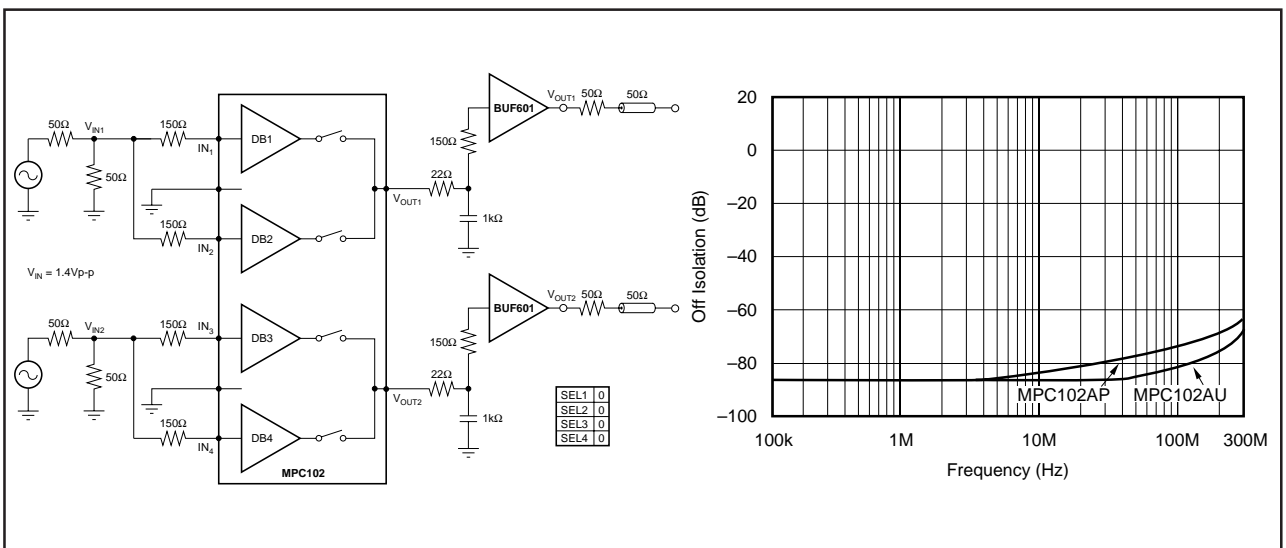


FIGURE 5. Off Isolation Test Circuit 2.

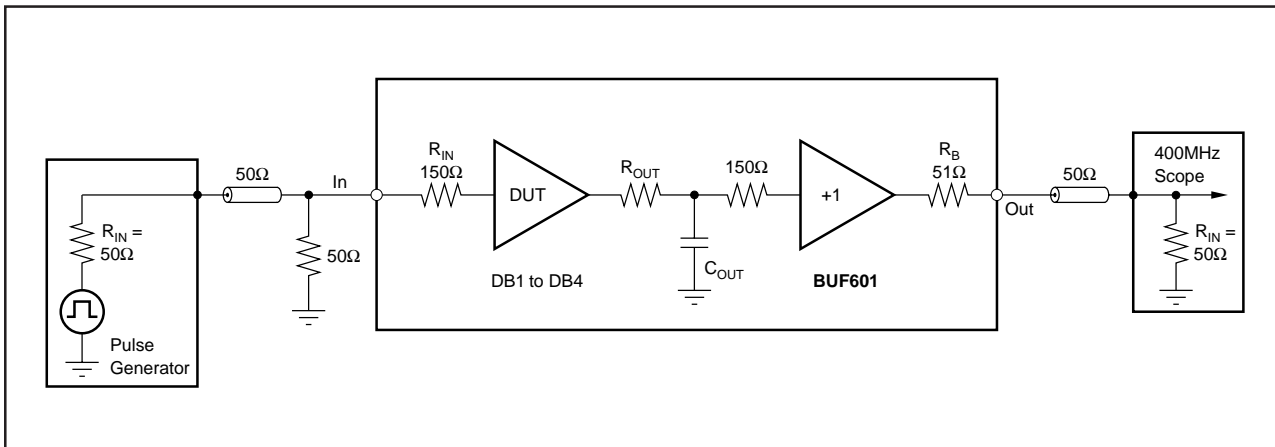


FIGURE 6. Test Circuit Pulse Response.

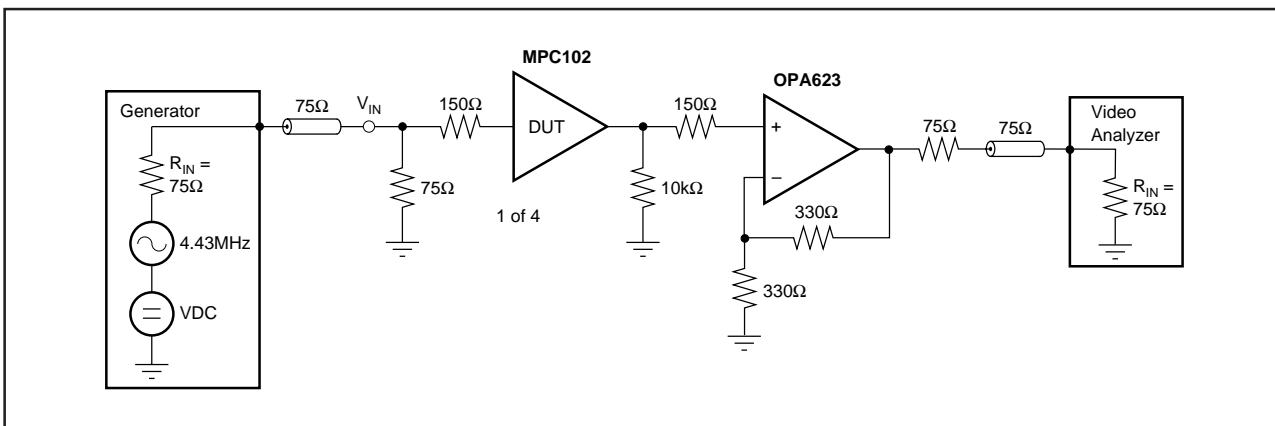


FIGURE 7. Test Circuit Differential Gain and Phase.

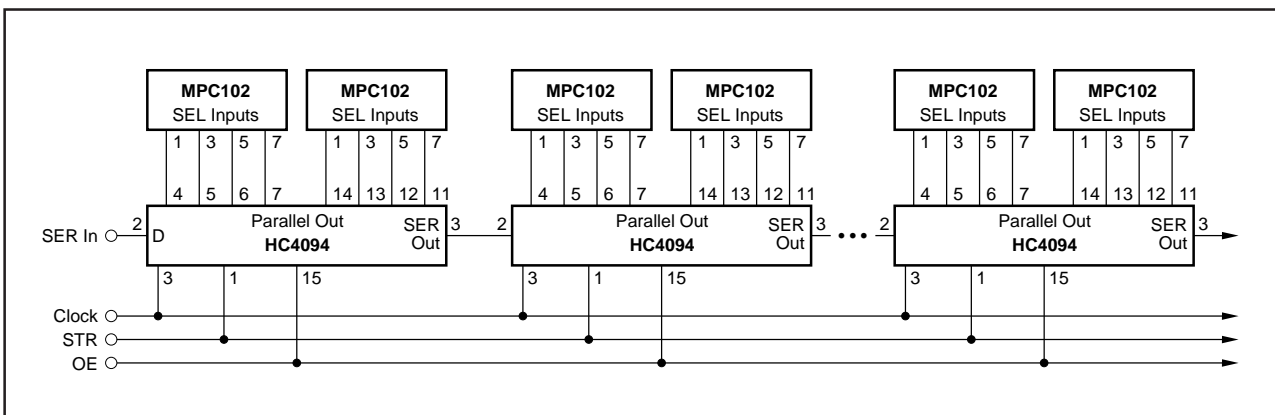


FIGURE 8. Serial Bus-Controlled Distribution Field.

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